GOP_XCR3064XL
USER'S MANUAL
V 0.9

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1. Table of contents:

1. Table of contents: 3
2. Introduction....5
2.1. GOP_ XCR3064XL Features: 5
2.2. GOP_XCR3064XL Applications: 5
2.3. Xilinx XCR3064XL CPLD Features:....6
2.4. Xilinx XCR3064XL CPLD Disadvantages:....6
2.5. GOP_XCR3064XL Board Picures, Top And Bottom View. 7
2.6. GOP_XCR3964XL Board In A Lab Environment.....8
3. GOP_XCR3964XL Board Overview 9
3.1. I/O Distribution....9
3.2. JTAG Port....10
Power Suppy....11
3.3. PAL / GAL Emulation Of 24 Pin And 20 Pin Devices 11
4. CPLD Design Support 12
5. GOP_XCR3064XL I/O Voltage Levels 13
6. Detailed XCR3064XL-10VQ44 CPLD Pinout Table 14
7. CON1 DIL Connector Pinout Table 17
8. CON4 Test Connector Pinout Table....18
9. CON3 Configuration Jumper options....18
10. DIL Connector Layout....19
11. Schematics 20
12. Module Layout Top View 21
13. Module Layout Bottom View....22
14. Technical Specifications....23
15. Literature....24
16. USER'S MANUAL Revisions....25

2. Introduction

The GOP_XCR3064XL is a mini module composed of a CPLD device with a PAL / GAL compatible 24 pin DIL footprint. Many additional features make it useful and flexible:

2.1. GOP_ XCR3064XL Features:

- XCR3064XL-10VQ44C CPLD, a member of the XILINX CoolRunner XPLA3 family, with a 24 or 20 pin PAL / GAL compatible DIL footprint
- Xilinx Parallel Cable IV or Platform USB compatible download connector 14pin / 2mm, an OHO-Elektronik low cost programmer is also availllable
- Operating voltage from 3,5V to 5,5V
- Serial resistors in the I/O and test connector pins helps to decrease ringing
- Onboard Clock oscillator with 49.152 MHz for audio or RS232 applications
- Reverse plug in protection
- A red / green dual led
- A 7-pin test connector for probing internal signals, or interconnecting several GOP's
- Solder jumpers for additional ground connections.
- Easy to reuse
- Professional design, manufactured on a 4 layer PCB, Made in Germany

2.2. GOP_XCR3064XL Applications:

- Replacement of PAL / GAL devices
- Rapid Prototyping
- Fast evaluation of Xilinx CPLD's
- Battery operated equipment
- Hardware platform for VHDL / VERILOG / digital design introductory courses

2.3. Xilinx XCR3064XL CPLD Features:

Document [1] and [2] lists lots of goodies, here are the best facts:

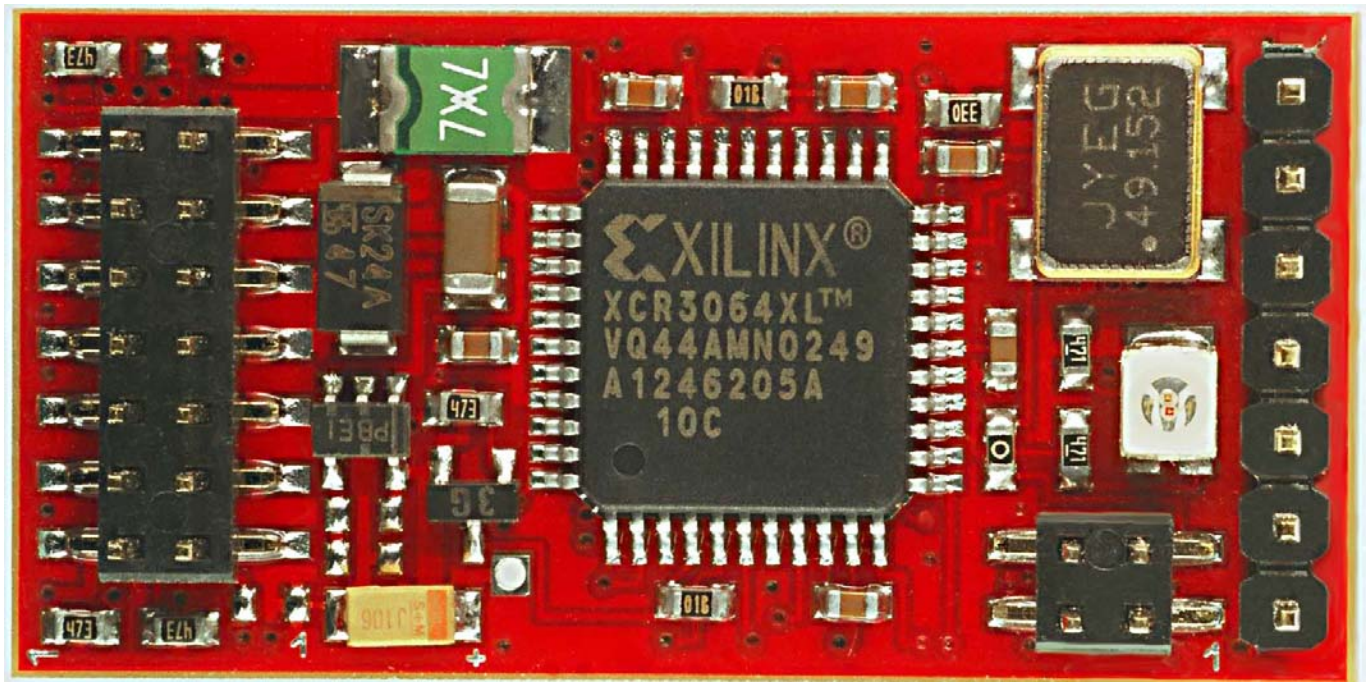
- Fast and modern low power CPLD, quiescent current is 18uA typ. at 25°C
- 4 logic arrays "16V40", each offers 40 array inputs with 16 macrocells and a 48 product term PLA
- Macrocells offer D ,T and Latch type memory elements with dedicated CE input, Flipflops can toggle on rising and falling edges, but not on both
- 4 global clocks and product term clock
- Inputs are 5V tolerant
- Input registers with little setup time of 2,5ns typ.
- JTAG port is multiplexed with user I/O, 36 I/O pins in a VQ44 package in contrast to 34 I/O's in other CPLD families with the same package
- Free powerful VHDL / VERILOG / schematics / simulation design software availlable (Webpack)
- 10000 reprogramming cycles, 20 years data retention
- Widely used CPLD, lots of information availlable by XILINX Inc. and on the web

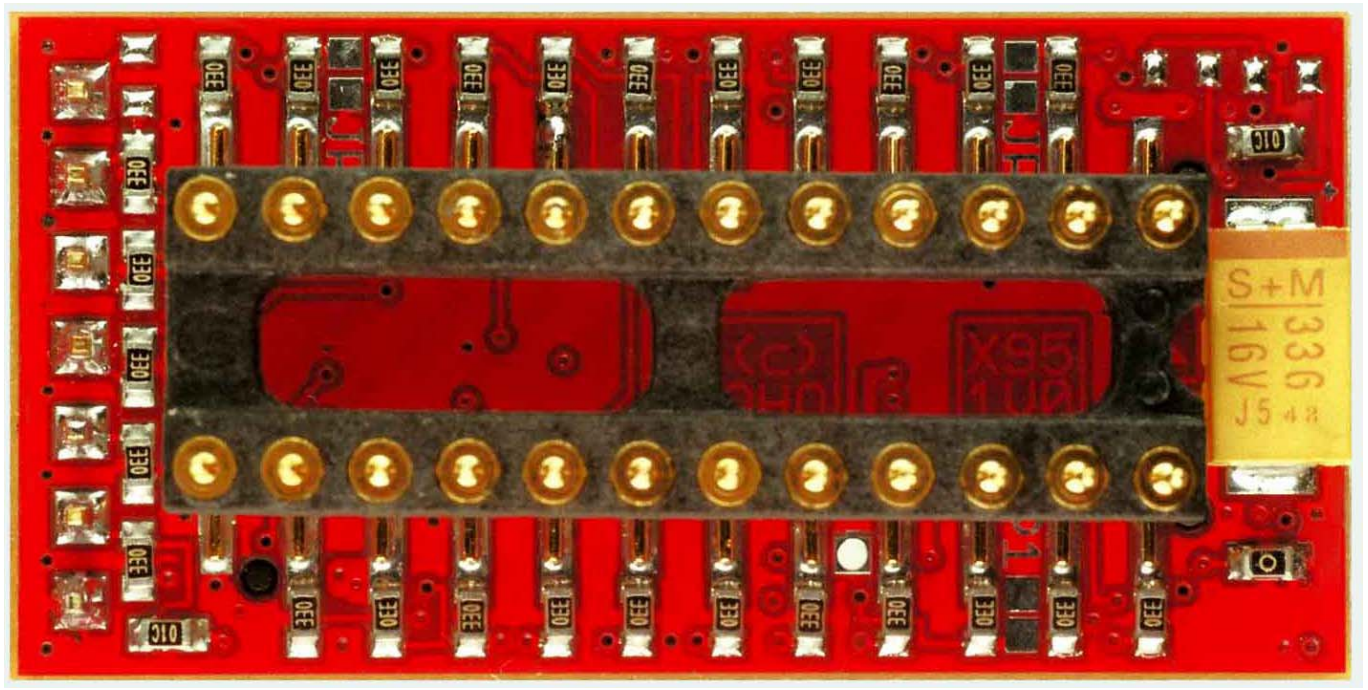
2.4. Xilinx XCR3064XL CPLD Disadvantages:

The following items are not relevant in most cases.
However they should be used as a checklist, wheather an application is affected.

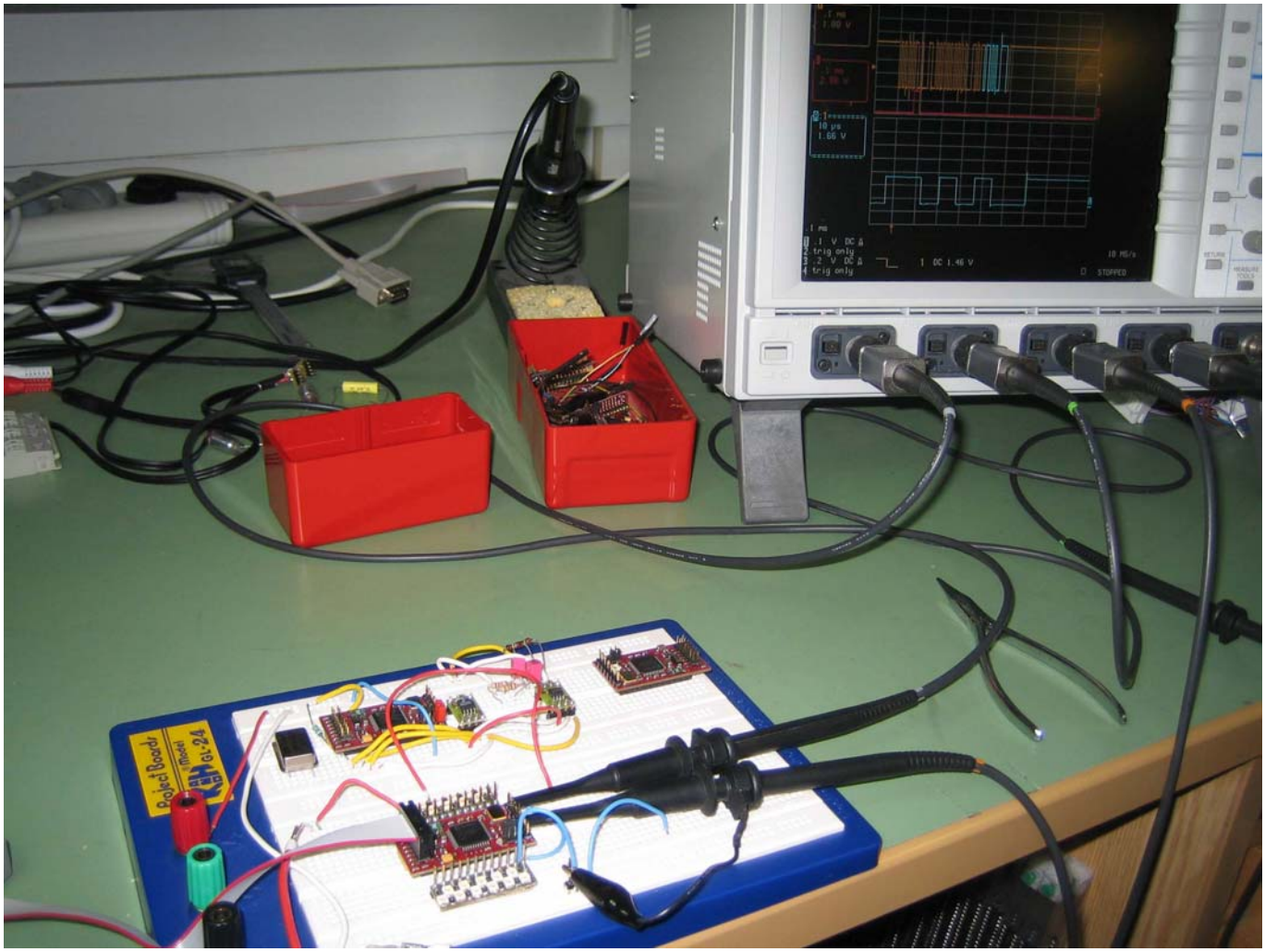
- Despite the PLA architecture, least amount of product terms per macrocell of all Xilinx CPLD families
- Flipflops can not clock on both edges like CoolRunner-II
- No global tristate net or set / reset net
- In rare cases, reprogramming is only possible, if no running clocks are applied to any CPLD pin

2.5. GOP_XCR3064XL Board Picures, Top And Bottom View.

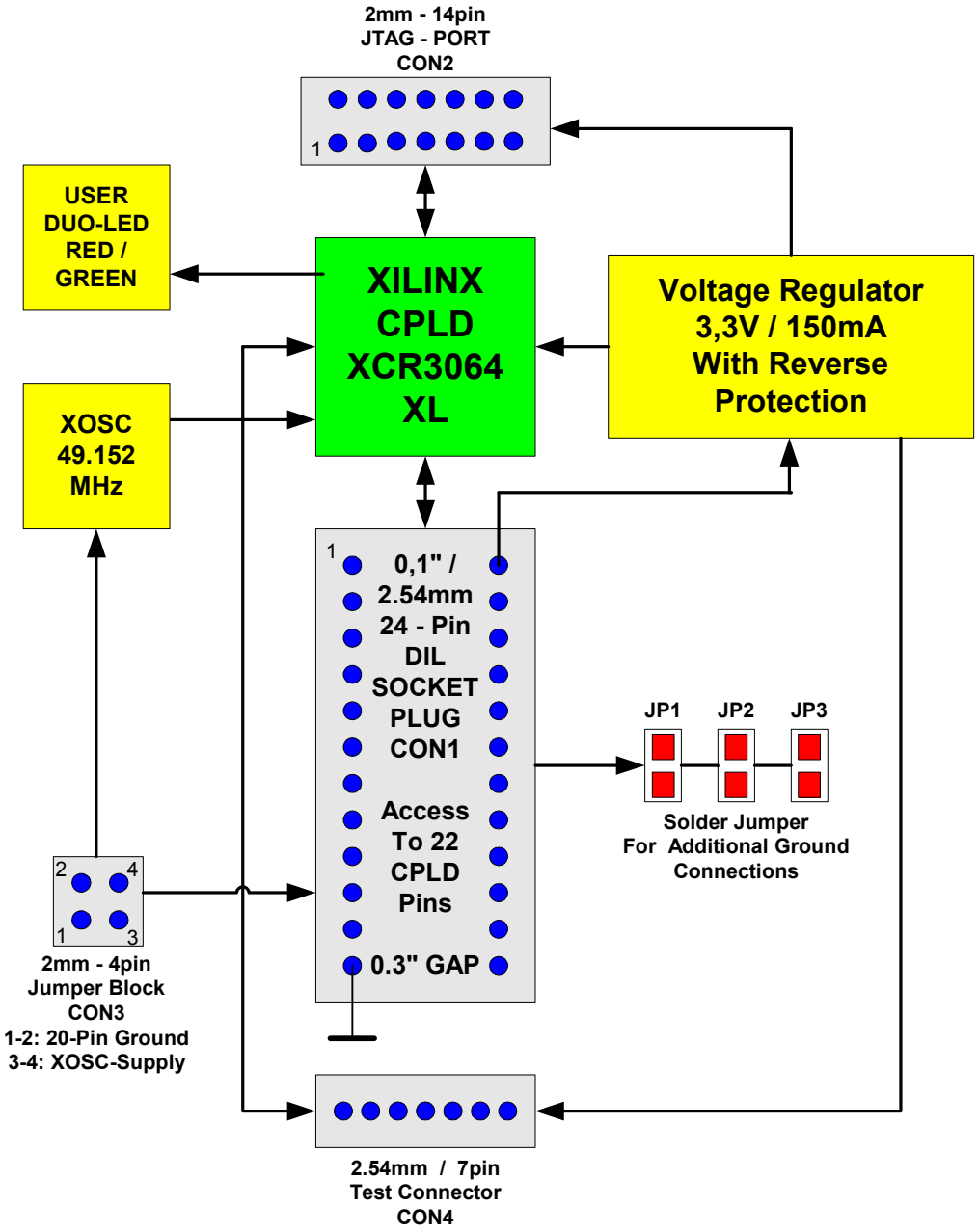




2.6. GOP_XCR3964XL Board In A Lab Environment.



3. GOP_XCR3964XL Board Overview



3.1. I/O Distribution

22 Xilinx XCR3064XL-10VQ44C CPLD I/O's are wired to a 24 pin DIL socket plug (CON1) on the bottom of the module through 22Ω serial resistors. These resistors primarily reduces ringing.

Pin 1 and 2 of the DIL plug accesses global clock nets CLK0 and CLK1 inside the CPLD.

5 remaining I/O's are availlable to the front side test connector CON4, also through 22Ω series resistors.

Pin 2 of CON4 has a pullup resistor to VCC (R40). A 2.54mm jumper can be used to short pin 2 to GND at pin 1 of the testconnector as a simple status input.

Pin 7 of the testconnector has an unmounted pullup resistor to the 5V supply voltage. If a 5V rails is needed on this pin, a resistor between 680Ω and 10kΩ could be soldered on position R46.
Please note, that 5V rails can be produced only by tristating outputs. A logical '1' output on an XCR3064XL is clamped to VCCIO, which is 3,3V on this module.

A crystal oscillator with an output frequency of 49,152MHz is connected to another I/O of the CPLD. This oscillator can be disabled completely by removing its power supply at jumper block CON3 position 3-4.
Please note, that this clock must be routed inside the CPLD to a global clock net, to insure proper synchronous circuit operation.

Furthermore 2 I/O's are connected to a dual led, having a red and a green chip in it's case. These leds can be lighted by driving a logical '1' to these I/O's.

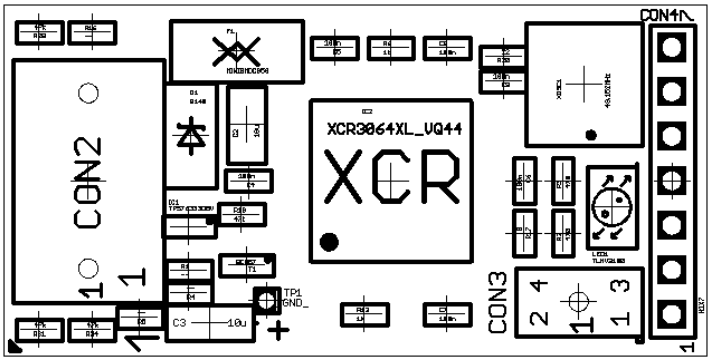
Finally 2 I/O's are connected to an RC network for demontration purpose.
A simple RC oscillator can be evaluated.
However it can be observed, that an XCR3xxx RC oscillator does't produce a stable clock.
If a global clock net wants to be accessed by a macrocell, removing of C8 of the RC filter is recommended.

3.2. JTAG Port

The CPLD JTAG signals are routed directly to the Xilinx standard 2mm 14pin JTAG port connector CON2, supported from the Parallel cable IV, and Platform USB cable, see [5], [6].
Pin 1 of the port is connected to GND, which allows high speed programming with the above cables.
Pins 12 and 14 of the JTAG port are not used on this module.

Pin 13 is used to enable the JTAG port of the CPLD. If this pin is low, the port is enabled.
Since the JTAG pins also can be I/O's, a logical high on pin 13 enables the GOP_XCR3064XL module to communicate with the PC with an SPI interface. Therefore an adaptor must be used between a download cable type III and the module, to set pin 13 to '1'.

Please notice the pin orientation of JTAG port CON2:



Power Suppy

The module can be powered at DIL pin 24 from 3,5 to 5,5 Volts.
Module GND pin is pin 12 in 24 pin mode, and pin 10 in 20 pin mode.
An onboard voltage regulator produces the CPLD core and I/O voltage of 3,3V.
The regulator [4] can source up to 150mA.

The module has a protection against reverse insertion, or reverse power connection.
In that case, the protection shorts the power supply by a polyfuse device.
The polyfuse recovers after deactivation of the power supply.
Burn through cycles of the polyfuse are limited.
For more information, please consult the data sheet.

Even so care should be taken when plugging the module.
Consider that a short pulse of several amps can damage the environment in which the module is inserted.

3.3. PAL / GAL Emulation Of 24 Pin And 20 Pin Devices

As a general hint, the DIL plug should be protected mechanically with the supplied DIL sockets as an adaptor.

In 24 pin mode of the module, a 24 pin socket should be used.

In 20 pin mode of the module, a 20 pin socket should be used.

Please insure, that pin 1 of the module is always pin 1 of a socket.

In the 20 pin mode, an additional GND connection must be done via a 2mm jumper on jumper block CON3 at position 1-2, see Layout Top View. This adds GND to pin 10.

In rare cases additional GND connections are desired.
Pins 3, 14 and 23 can be shorted to GND with solder jumpers JP1, JP3, JP2 respectively, on the bottom side of the module. These shorts should be soldered via a stereo microscope, to insure, that there are no other invalid connections.

4. CPLD Design Support

As for CPLD design [3] and [8] are very recommended readings.

VHDL and UCF design templates for 20 and 24 pin configurations are availlable.

5. GOP_XCR3064XL I/O Voltage Levels

Since CPLD I/O's can be inputs or outputs or bidirectional, we have to distinguish between voltage levels driven from the outputs of the CPLD, and voltage levels that are applied to their inputs.

The XCR3xxx XPLA3 series inputs can accept input voltage levels from 0 to 5V, so they are 5V tolerant.
However they can not deal with analog input voltages.
The maximum low input voltage VIL, where the CPLD sees a logical '0', must be 0.8V.
The minimum high input voltage VIH, where the CPLD sees a logical '1', must be 2.0V, and must not exceed 5,5V.
Voltage levels in between VIL and VIH should change very fast, transition times should be lower than 100ns, although Xilinx makes no recommendations about them in this CPLD family.

Unused I/O pins always have an enabled internal pullup, see [10].
Buskeepers are not availlable on this CPLD family.

It is remarkable, that because of the 5V tolerant inputs, there is no diode between the inputs and VCC. So the devices can be used in hot plugging applications.

The XCR3xxxXL series outputs delivers 2,7V - 3,3V voltage levels only.
The GOP_XCR3064XL module supports 3,3V only.
The CPLD drives a low output '0' with a maximum of 0,4V at 8mA sink current.
If the CPLD sources current on a logical '1' output, the voltage is guaranteed to be 2,4V minimum at 8mA.
So sourcing and sinking current is symmetrical.
If more output current is desired, [7] shows appropriate I/V curves.

Another important fact is, that a bidirectional I/O with a pullup to 5V, can not drive to 5V on the output, but 3,3V only. The output driver stage clamps the voltage to VCCIO in that case.

As an example, driving bright leds with relatively high current consumption is best done by sinking current, or in other words, the cathode of the led should be connected to a CPLD I/O, the anode to the led's supply voltage.
If the leds have forward voltages beyond 3,3V (e.g. blue leds) , the 5V tolerance can be used to completely turn off the led by tristating the output.
For driving leds with CPLD's, see also [9].

Please consider that there are 22Ω series resistors between GOP_XCR3064XL pin connections and the CPLD.

6. Detailed XCR3064XL-10VQ44 CPLD Pinout Table

Pin	CPLD pin function *	(Schema net name) routed to	UCF port 24pin** (20 pin)	1. Comment:
1	FB2MC9 TDI	(TDI)	ptdi	Dual function pin, JTAG port TDI or user I/O If PORT_EN = 1, force JTAG port, otherwise user I/O
2	FB2MC10	(PLD2) CON1 pin4	pin4 (pin4)	Connection to the 20/24pin DIL plug to pin4 via serial resistor
3	FB2MC11	(PLD3) CON1 pin7	pin5 (pin5)	Connection to the 20/24pin DIL plug to pin5 via serial resistor
4	PORT_EN	(PORT_EN)	--	If PORT_EN = 1, force JTAG port, otherwise user I/O
5	FB2MC14	(PLD5) CON1 pin6	pin6 (pin6)	Connection to the 20/24pin DIL plug to pin6 via serial resistor
6	FB2MC15	(PLD6) CON1 pin8	pin7 (pin7)	Connection to the 20/24pin DIL plug to pin7 via serial resistor
7	FB4MC1 TMS	(TDI)	ptms	Dual function pin, JTAG port TMS or user I/O If PORT_EN = 1, force JTAG port, otherwise user I/O
8	FB4MC2	(PLD8) CON1 pin11	pin11 (--)	Connection to the 24pin DIL plug to pin11 via serial resistor Not used for the 20pin DIL plug
9	VCC	Power VCC	--	Power supply 3,3V from regulator TPS76333
10	FB4MC4	(PLD10) CON1 pin8	pin8 (pin8)	Connection to the 20/24pin DIL plug to pin8 via serial resistor
11	FB4MC5	(PLD11) CON1 pin9	pin9 (pin9)	Connection to the 20/24pin DIL plug to pin9 via serial resistor
12	FB4MC9	(PLD12) CON1 pin10	pin10 (--)	Connection to the 24pin DIL plug to pin10 via serial resistor Short to GND by CON3 for 20pin DIL plug
13	FB4MC10	(PLD13) CON4 pin2	tp2	Test connector pin2
14	FB4MC11	(PLD14) CON4 pin3	tp3	Test connector pin3
15	FB4MC12	(LED_R) CON4 pin4	tp4	Test connector pin4 Red led of the duo led 0 -> led off, 1 -> led on
16	GND	Power GND	--	Connection to the GND Layer of the PCB
17	VCC	Power VCC	--	Power supply 3,3V from regulator TPS76333
18	FB3MC13	(LED_G) CON4 pin4	tp5	Test connector pin5 Green led of the duo led 0 -> led off, 1 -> led on
19	FB3MC12	(PLD19) CON4 pin6	tp6	Test connector pin6 R46 could be soldered to the 5V supply voltage, for generation of an 5V rail on tp6. Use 680Ω to 10kΩ.
20	FB3MC11	(PLD20) CON1 pin13	pin13 (--)	Connection to the 24pin DIL plug to pin13 via serial resistor Not used for the 20pin DIL plug
21	FB3MC10	(PLD21) CON1 pin14	pin14 (--)	Connection to the 24pin DIL plug to pin14 via serial resistor Not used for the 20pin DIL plug
22	FB3MC9	(PLD22) CON1 pin15	pin15 (pin11)	Connection to the 24pin DIL plug to pin15 via serial resistor Connection to the 20pin DIL plug to pin11 via serial

				resistor
23	FB3MC4	(PLD23) CON1 pin16	pin16 (pin12)	Connection to the 24pin DIL plug to pin16 via serial resistor Connection to the 20pin DIL plug to pin12 via serial resistor
24	GND	Power GND	--	Connection to the GND Layer of the PCB
25	FB3MC2	(PLD25) CON1 pin17	pin17 (pin13)	Connection to the 24pin DIL plug to pin17 via serial resistor Connection to the 20pin DIL plug to pin13 via serial resistor
26	FB3MC1 TCK	(TCK)	ptck	Dual function pin, JTAG port TCK or user I/O If PORT_EN = 1, force JTAG port, otherwise user I/O
27	FB1MC15	(PLD27) CON1 pin18	pin18 (pin14)	Connection to the 24pin DIL plug to pin18 via serial resistor Connection to the 20pin DIL plug to pin14 via serial resistor
28	FB1MC14	(RC_IN) RC network	rcin	Input to an RC network, this is for demonstration, that rc oscillators do not work reliably with XCR3064XL, but on CoolRunner-II devices with Schmitt Trigger inputs.
29	VCC	Power VCC	--	Power supply 3,3V from regulator TPS76333
30	FB1MC11	(PLD30) CON1 pin19	pin19 (pin15)	Connection to the 24pin DIL plug to pin19 via serial resistor Connection to the 20pin DIL plug to pin15 via serial resistor
31	FB1MC10	(PLD31) CON1 pin20	pin20 (pin16)	Connection to the 24pin DIL plug to pin20 via serial resistor Connection to the 20pin DIL plug to pin16 via serial resistor
32	FB1MC9 TDO	(TDO)	ptdo	Dual function pin, JTAG port TDO or user I/O If PORT_EN = 1, force JTAG port, otherwise user I/O
33	FB1MC8	(PLD33) CON1 pin21	pin21 (pin17)	Connection to the 24pin DIL plug to pin21 via serial resistor Connection to the 20pin DIL plug to pin17 via serial resistor
34	FB1MC2	(PLD34) CON1 pin22	pin22 (pin18)	Connection to the 24pin DIL plug to pin22 via serial resistor Connection to the 20pin DIL plug to pin18 via serial resistor
35	FB1MC1	(PLD35) CON1 pin23	pin23 (pin19)	Connection to the 24pin DIL plug to pin23 via serial resistor Connection to the 20pin DIL plug to pin19 via serial resistor
36	GND	Power GND	--	Connection to the GND Layer of the PCB
37	IN3/CLK3	(OSC) XOSC1	osc	Crystal oscillator input to global clock net CLK3
38	IN2/CLK2	(RC_OUT) RC network	rcout	Output from an RC network, this is for demonstration, that rc oscillators do not work reliably with XCR3064XL, but on CoolRunner-II devices with Schmitt Trigger inputs
39	IN1/CLK1	(PLD43) CON1 pin2	pin2 (pin2)	Connection to the 20/24pin DIL plug to pin2 via serial resistor Access to global clock net CLK1
40	IN0/CLK0	(PLD42) CON1 pin1	pin1 (pin1)	Connection to the 20/24pin DIL plug to pin1 via serial resistor Access to global clock net CLK0
41	VCC	Power VCC	--	Power supply 3,3V from regulator TPS76333

42	FB2MC16	(PLD42) CON1 pin1	pin1 (pin1)	Connection to the 20/24pin DIL plug to pin1 via serial resistor Access to global clock net CLK0
43	FB2MC2	(PLD43) CON1 pin2	pin2 (pin2)	Connection to the 20/24pin DIL plug to pin2 via serial resistor Access to global clock net CLK1
44	FB2MC3	(PLD44) CON1 pin3	pin3 (pin3)	Connection to the 20/24pin DIL plug to pin3 via serial resistor

* FB1MC11 denotes function block1, macrocell 11
** There is an UCF file definition for 24pin, and another one for 20pin device usage

7. CON1 DIL Connector Pinout Table

Pin	CPLD pin function *	(Schema net name) routed to	UCF port name **	Comment
1	FB2MC16	(PLD42) CON1 pin1	pin1 (pin1)	Connection to the 20/24pin DIL plug to pin1 via serial resistor Access to global clock net CLK0
2	FB2MC2	(PLD43) CON1 pin2	pin2 (pin2)	Connection to the 20/24pin DIL plug to pin2 via serial resistor Access to global clock net CLK1
3	FB2MC3	(PLD44) CON1 pin3	pin3 (pin3)	Connection to the 20/24pin DIL plug to pin3 via serial resistor
4	FB2MC10	(PLD2) CON1 pin4	pin4 (pin4)	Connection to the 20/24pin DIL plug to pin4 via serial resistor
5	FB2MC11	(PLD3) CON1 pin7	pin5 (pin5)	Connection to the 20/24pin DIL plug to pin5 via serial resistor
6	FB2MC14	(PLD5) CON1 pin6	pin6 (pin6)	Connection to the 20/24pin DIL plug to pin6 via serial resistor
7	FB2MC15	(PLD6) CON1 pin8	pin7 (pin7)	Connection to the 20/24pin DIL plug to pin7 via serial resistor
8	FB4MC4	(PLD10) CON1 pin8	pin8 (pin8)	Connection to the 20/24pin DIL plug to pin8 via serial resistor
9	FB4MC5	(PLD11) CON1 pin9	pin9 (pin9)	Connection to the 20/24pin DIL plug to pin9 via serial resistor
10	FB4MC9	(PLD12) CON1 pin10	pin10 (--)	Connection to the 24pin DIL plug to pin10 via serial resistor Short to GND by CON3 for 20pin DIL plug
11	FB4MC2	(PLD8) CON1 pin11	pin11 (--)	Connection to the 24pin DIL plug to pin11 via serial resistor Not used for the 20pin DIL plug
12	GND	GND	--	Power ground plane connection
13	FB3MC11	(PLD20) CON1 pin13	pin13 (--)	Connection to the 24pin DIL plug to pin13 via serial resistor Not used for the 20pin DIL plug
14	FB3MC10	(PLD21) CON1 pin14	pin14 (--)	Connection to the 24pin DIL plug to pin14 via serial resistor Not used for the 20pin DIL plug
15	FB3MC9	(PLD22) CON1 pin15	pin15 (pin11)	Connection to the 24pin DIL plug to pin15 via serial resistor Connection to the 20pin DIL plug to pin11 via serial resistor
16	FB3MC4	(PLD23) CON1 pin16	pin16 (pin12)	Connection to the 24pin DIL plug to pin16 via serial resistor Connection to the 20pin DIL plug to pin12 via serial resistor
17	FB3MC2	(PLD25) CON1 pin17	pin17 (pin13)	Connection to the 24pin DIL plug to pin17 via serial resistor Connection to the 20pin DIL plug to pin13 via serial resistor
18	FB1MC15	(PLD27) CON1 pin18	pin18 (pin14)	Connection to the 24pin DIL plug to pin18 via serial resistor Connection to the 20pin DIL plug to pin14 via serial resistor
19	FB1MC11	(PLD30) CON1 pin19	pin19 (pin15)	Connection to the 24pin DIL plug to pin19 via serial resistor Connection to the 20pin DIL plug to pin15 via serial resistor
20	FB1MC10	(PLD31) CON1 pin20	pin20 (pin16)	Connection to the 24pin DIL plug to pin20 via serial resistor Connection to the 20pin DIL plug to pin16 via serial resistor
21	FB1MC8	(PLD33) CON1 pin21	pin21 (pin17)	Connection to the 24pin DIL plug to pin21 via serial resistor Connection to the 20pin DIL plug to pin17 via serial resistor
22	FB1MC2	(PLD34) CON1 pin22	pin22 (pin18)	Connection to the 24pin DIL plug to pin22 via serial resistor Connection to the 20pin DIL plug to pin18 via serial resistor
23	FB1MC1	(PLD35)	pin23	Connection to the 24pin DIL plug to pin23 via serial resistor

		CON1 pin23	(pin19)	Connection to the 20pin DIL plug to pin19 via serial resistor
24	--	PIN_24	--	5V input voltage to the module

8. CON4 Test Connector Pinout Table

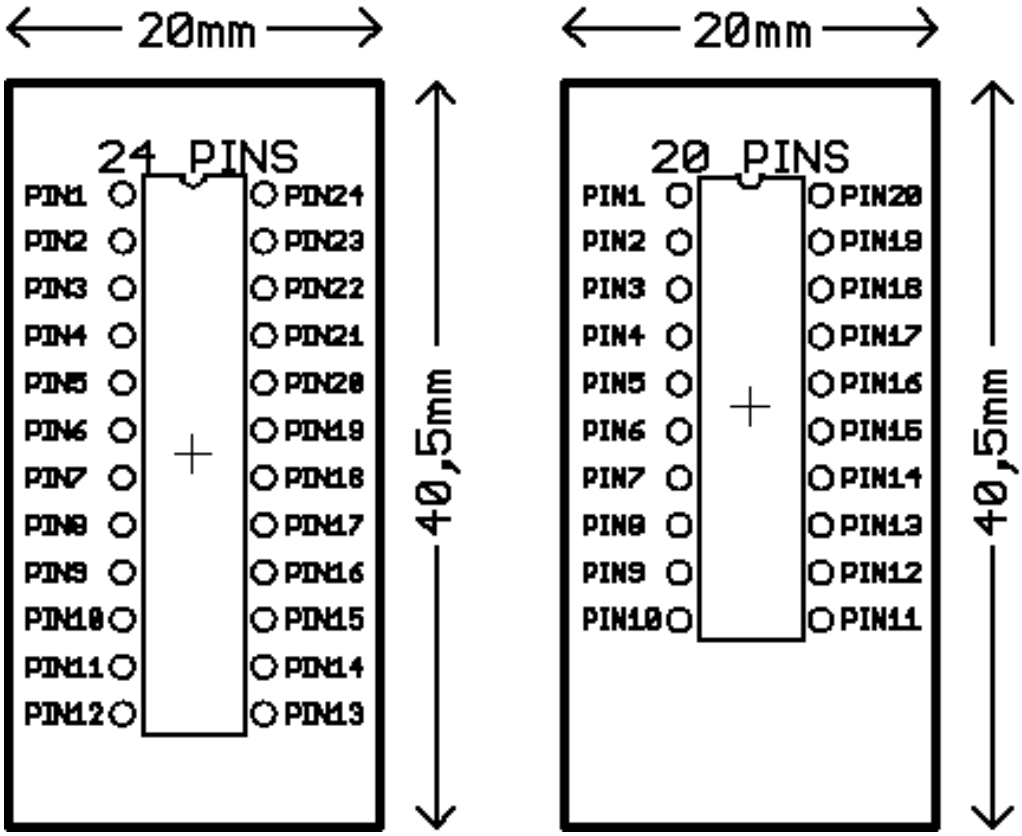
Pin	CPLD pin function *	(Schema net name) routed to	UCF port name **	Comment
1	GND	GND	--	Power ground plane connection
2	FB4MC10	(PLD13) CON4 pin2	tp2	Test connector pin2
3	FB4MC11	(PLD14) CON4 pin3	tp3	Test connector pin3
4	FB4MC12	(LED_R) CON4 pin4	tp4	Test connector pin4 Red led of the duo led 0 -> led off, 1 -> led on
5	FB3MC13	(LED_G) CON4 pin4	tp5	Test connector pin5 Green led of the duo led 0 -> led off, 1 -> led on
6	FB3MC12	(PLD19) CON4 pin6	tp6	Test connector pin6 R46 could be soldered to the 5V supply voltage, for generation of an 5V rail on tp6. Use 680Ω to 10kΩ.
7	--	(VCC_IN) PIN24	--	5V input voltage protected by a polyfuse

9. CON3 Configuration Jumper options

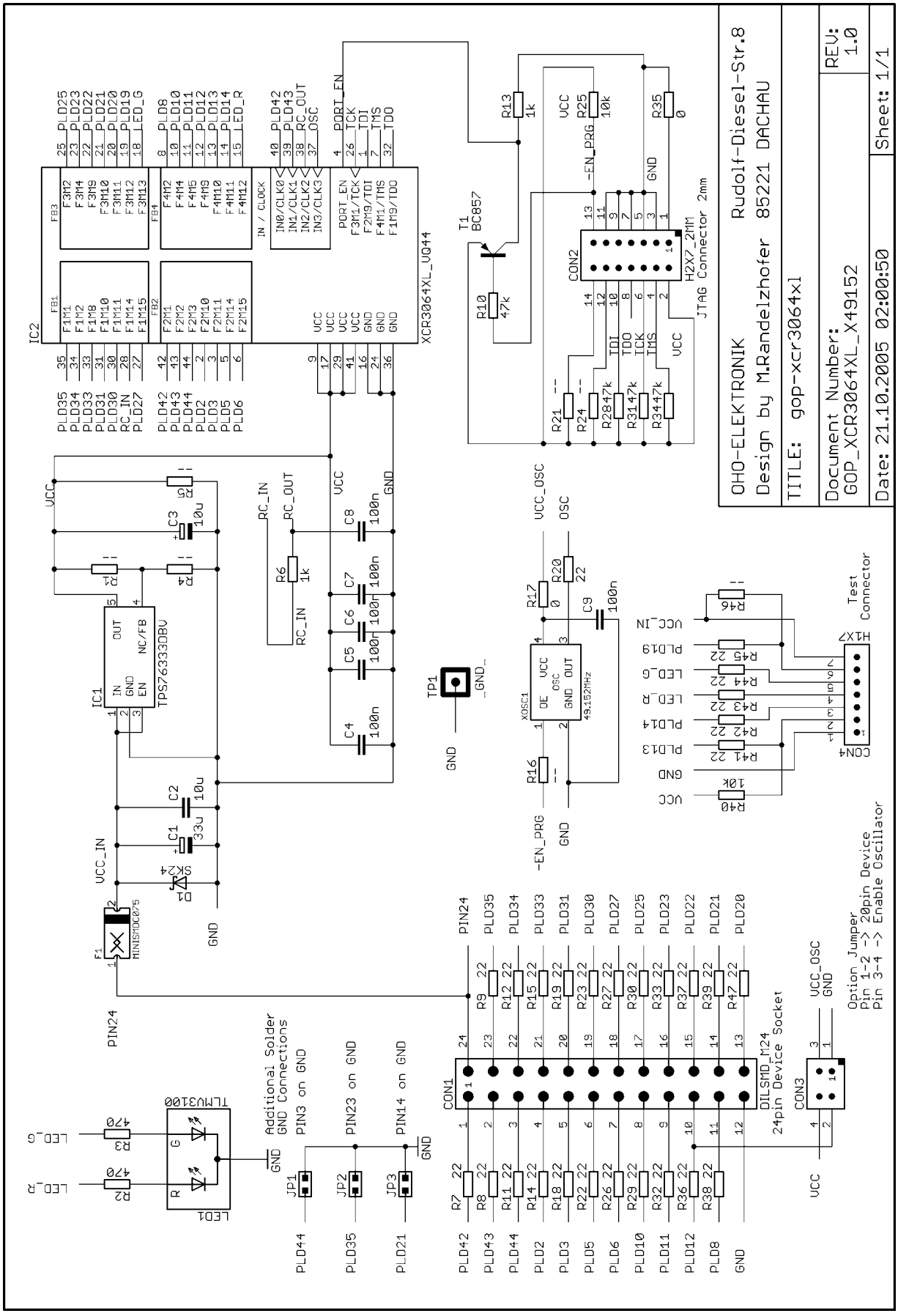
1-2	Enable 20pin PAL / GAL Emulation, put GND to pin 10 of CON1
3-4	Enable XOSC1 crystal oscillator 49,152 MHz

10. DIL Connector Layout

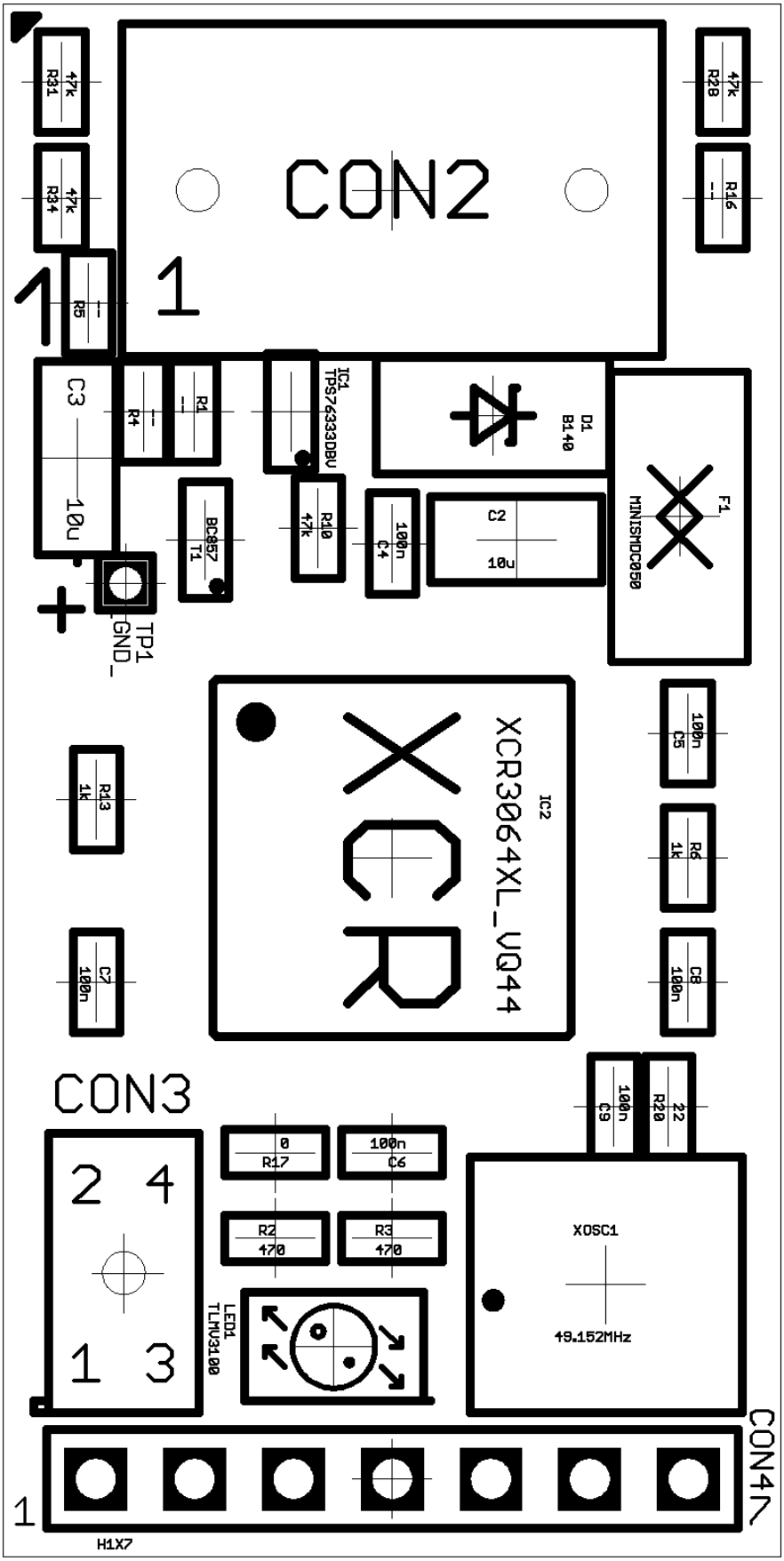
GOP_XCR3064XL module top view for 24 pin and 20 pin emulation mode:



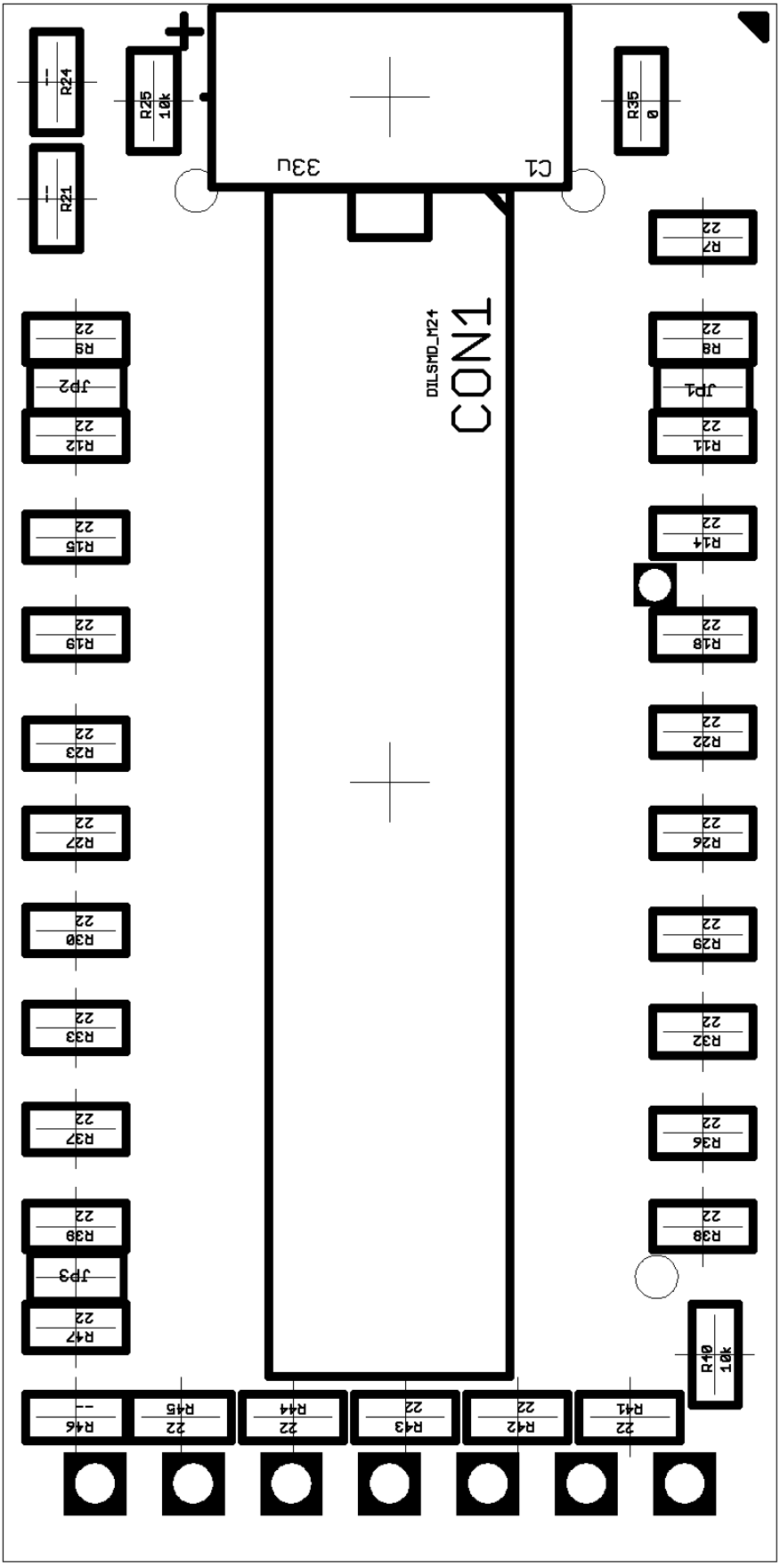
11. Schematics



12. Module Layout Top View



13. Module Layout Bottom View



14. Technical Specifications

CPLD:	Xilinx XCR3064XL-10VQ44C
Supply Voltage on PIN24:	3,5 - 5,5V
Size:	40,5 x 20mm, 1,594" x 0,787"
Height PCB to Top:	max. 8mm, 0,315"
Height PCB to Bottom:	max. 12mm, 0,472"
Weight:	7g

15. Literature

- [1] DS012 CoolRunner XPLA3 CPLD Family
  http://direct.xilinx.com/bvdocs/publications/ds012.pdf
- [2] DS017 XCR3064XL: 64 Macrocell CoolRunner CPLD
  http://direct.xilinx.com/bvdocs/publications/ds017.pdf
- [3] XAPP444 CPLD Fitting, Tips and Tricks
  http://direct.xilinx.com/bvdocs/appnotes/xapp444.pdf
- [4] TPS76333 Low Power 150mA Low Dropout Linear Regulators
  http://focus.ti.com/lit/ds/symlink/tps76333.pdf
- [5] DS097 Xilinx Parallel Cable IV
  http://direct.xilinx.com/bvdocs/publications/ds097.pdf
- [6] DS300 Platform Cable USB
  http://direct.xilinx.com/bvdocs/publications/ds300.pdf
- [7] XAPP150 I/V Curves for Xilinx FPGA and CPLD Families
  http://direct.xilinx.com/bvdocs/appnotes/xapp150.pdf
- [8] XAPP784 Bulletproof CPLD Design Practices
  http://direct.xilinx.com/bvdocs/appnotes/xapp784.pdf
- [9] XAPP805 Driving Leds with Xilinx CPLD's
  http://direct.xilinx.com/bvdocs/appnotes/xapp805.pdf
- [10] XAPP342 XPLA3 I/O Cell Characteristics
  http://direct.xilinx.com/bvdocs/appnotes/xapp342.pdf

16. USER'S MANUAL Revisions

Version	Date	Comments
V0.9	23/10/2005	Prerelease