GOP_XC9572XL
USER'S MANUAL
V 0.9

OHO-Elektronik
www.oho-elektronik.de

Author: M.Randelzhofer

OHO-Elektronik
Michael Randelzhofer

Rudolf-Diesel-Str. 8
85221 Dachau
Germany

WEB: www.oho-elektronik.de
EMAIL: info@oho-elektronik.de

Phone: +49 8131 339230
FAX: +49 8131 339294

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1. Table of contents:

2. Introduction

The GOP_XC9572XL is a mini module composed of a CPLD device with a PAL / GAL compatible 24 pin DIL footprint. Many additional features make it useful and flexible:

2.1. GOP_XC9572XL Features:

- ➢ XC9572XL-10VQ44C CPLD, a member of the XILINX XC9500XL family, with a 24 or 20 pin PAL / GAL compatible DIL footprint

- ➢ Xilinx Parallel Cable IV or Platform USB compatible download connector 14pin / 2mm, an OHO-Elektronik low cost programmer is also availlable

- ➢ Operating voltage from 3,5V to 5.5V

- ➢ Serial resistors in the I/O and test connector pins helps to decrease ringing

- ➢ Onboard Clock oscillator with 49.152 MHz for audio or RS232 applications

- ➢ Reverse plug in protection

- ➢ A red / green dual led

- ➢ A 7-pin test connector for probing internal signals, or interconnecting several GOP's

- ➢ Solder jumpers for additional ground connections.

- ➢ Easy to reuse

- ➢ Professional design, manufactured on a 4 layer PCB, Made in Germany

2.2. GOP_XC9572XL Applications:

- ➢ Replacement of PAL / GAL devices

- ➢ Rapid Prototyping

- ➢ Fast evaluation of Xilinx CPLD's

- ➢ Hardware platform for VHDL / VERILOG / digital design introductory courses

2.3. Xilinx XC9572XL CPLD Features:

Document [1] and [2] lists lots of goodies, here are the best facts:

➢ Highest density and lowest cost non volatile CPLD device in the 64 macrocell device class, but with 72 macrocells

➢ 4 logic arrays "18V54", each offers 54 (!) array inputs with 18 macrocells and 90 product terms, wired together by a FASTCONNECT II SWITCHMATRIX

➢ Inputs are 5V-tolerant

➢ Macrocells offer D and T type flipflops with dedicated CE input

➢ 3 global clocks, 2 global tristate nets and a global set / reset net

➢ Programmable ground I/O pins decreases ground bounce problems

➢ Free powerful VHDL / VERILOG / schematics / simulation design software availlable (Webpack)

➢ 10000 reprogramming cycles, 20 years data retention

➢ Widely used CPLD, lots of information availlable by XILINX Inc. and on the web

2.4. Xilinx XC9572XL CPLD Disadvantages:

The following items are not relevant in most cases.
However they should be used as a checklist, wheather an application is affected.

➢ Relative high power consumption

➢ Output current driving capability is asymmetrical: VOH: -4 mA, VOL: 8 mA in a 3,3V VCCIO configuration

➢ Inputs do not have sufficient hysteresis for Schmitt Trigger functionality, simple rc-oscillators won't work

➢ Relatively unflexible product term distribution (no PLA structure)

➢ Output voltages drives only up to VCCIO, a pullup can not reach 5V, except in tristate

➢ No input registers, I/O setup time is 6,5ns for XC9572XL-10 parts

➢ In rare cases, reprogramming is only possible, if no running clocks are applied to any CPLD pin

> ➢ Flipflops can trigger on positive or negative edges only, not on both. This is a feature found on CoolRunner-II devices only.

> ➢ No pullup option on the I/O's after configuration, but buskeepers

> ➢ Only 2 I/O standards: 3,3V and 2.5V, low 2.5V output drive capability

2.5. GOP_XC9572XL Board Picures, Top And Bottom View.
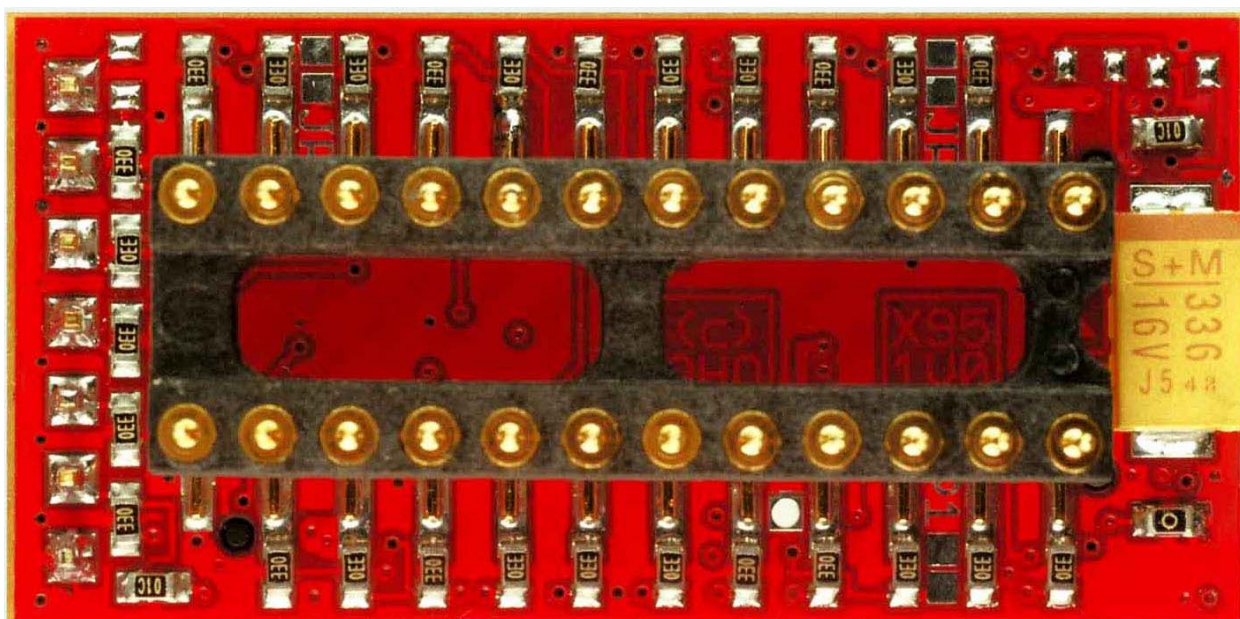
2.6.   GOP_XC9572XL Board In A Lab Environment.
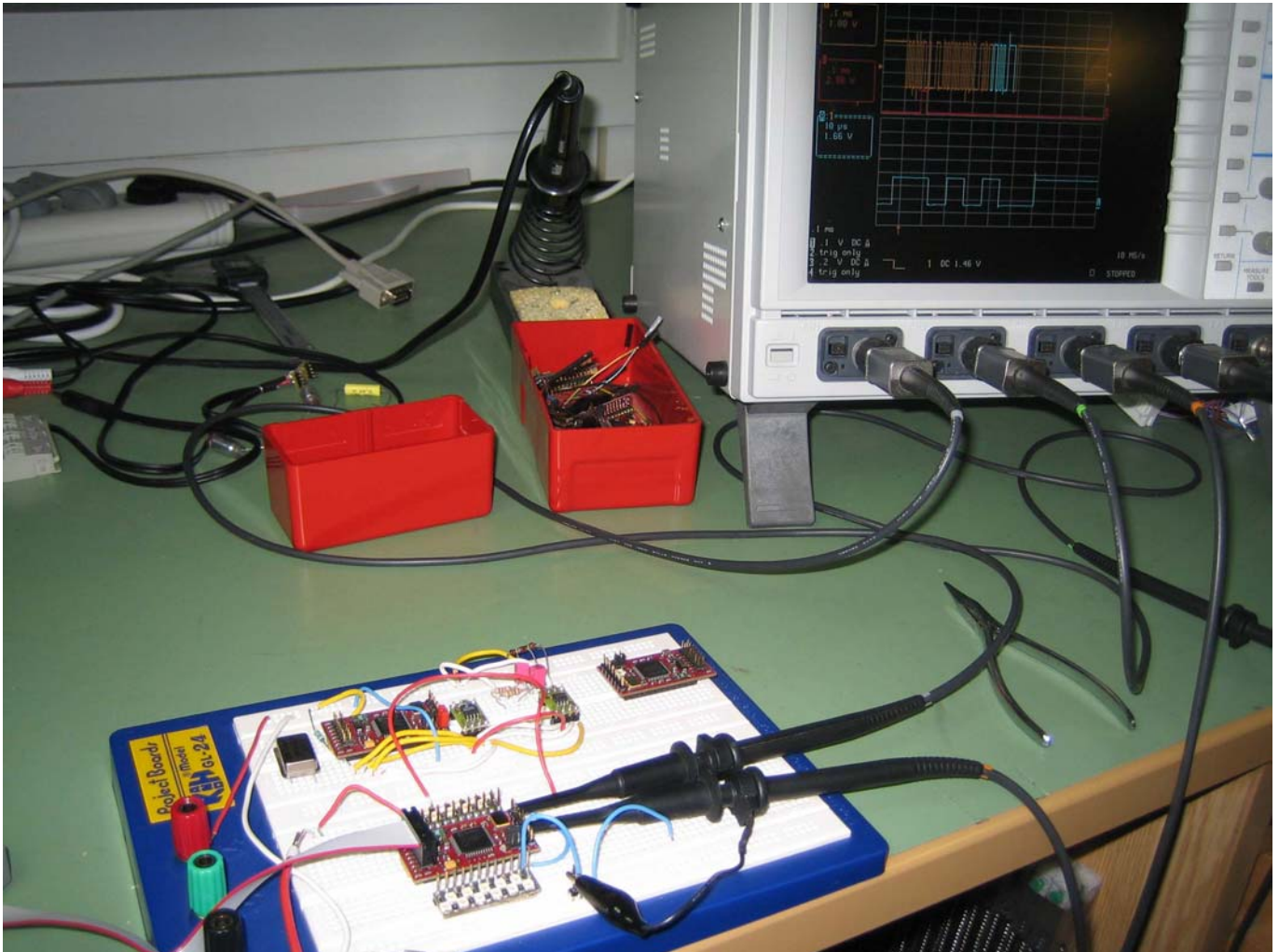
3. GOP_XC9572XL Board Overview
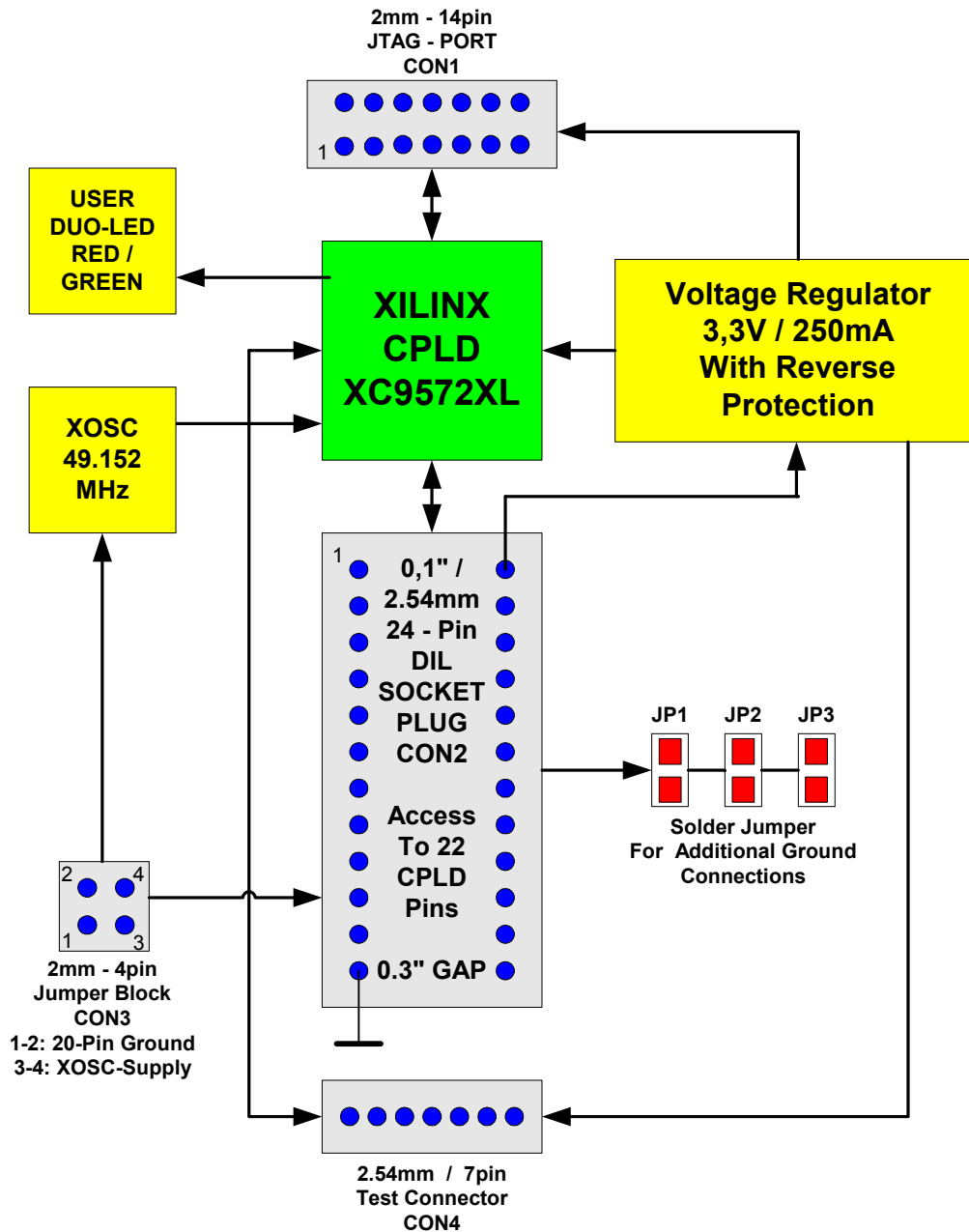
3.1. I/O Distribution

22 Xilinx XC9572XL-10VQ44C CPLD I/O's are wired to a 24 pin DIL socket plug (CON2) on the bottom of the module through 22Ω serial resistors. These resistors primarily reduces ringing.

Pin 1 and 2 of the DIL plug accesses global clock nets GCK1 and GCK2 inside the CPLD.
Pin 13 accesses the global tristate net GTS1.

5 remaining I/O's are availlable to the front side test connector CON4, also through 22Ω series resistors.
Pin 2 of the connector accesses the global tristate net GTS2.

This pin also has a pullup resistor to VCC (R39). A 2.54mm jumper can be used to short pin 2 to GND at pin 1 of the testconnector as a simple status input.

Pin 7 of the testconnector has an unmounted pullup resistor to the 5V supply voltage. If a 5V rails is needed on this pin, a resistor between 680Ω and 10kΩ could be soldered on position R44.

Please note, that 5V rails can be produced only by tristating outputs. A logical '1' output on an XC9572XL is clamped to VCCIO, which is 3,3V on this module.

A crystal oscillator with an output frequency of 49,152MHz is connected to another I/O of the CPLD. This oscillator can be disabled completely by removing its power supply at jumper block CON3 position 3-4.

Please note, that this clock must be routed inside the CPLD to a global clock net, to insure proper synchronous circuit operation.

Furthermore 2 I/O's are connected to a dual led, having a red and a green chip in it's case. These leds can be lighted by driving a logical '1' to these I/O's.

Finally 2 I/O's are connected to an RC network for demontration purpose.
A simple RC oscillator can be evaluated.
However it can be observed, that an XC95xxx RC oscillator does't produce a stable clock.
The same PCB is used for the CoolRunner-II module where the RC oscillator works fine due to selectable Schmitt Trigger inputs.
For the same reason CPLD pin 7 is fixed to GND, this is a compatibility issue to the CoolRunner-II module.

3.2. JTAG Port

The CPLD JTAG signals are routed directly to the Xilinx standard 2mm 14pin JTAG port connector CON1, supported from the Parallel cable IV, and Platform USB cable, see [7], [8].
Pin 1 of the port is connected to GND, which allows high speed programming with the above cables.
Pins 12,13 and 14 of the JTAG port are not used on this module.
Please notice the pin orientation of JTAG port CON1:
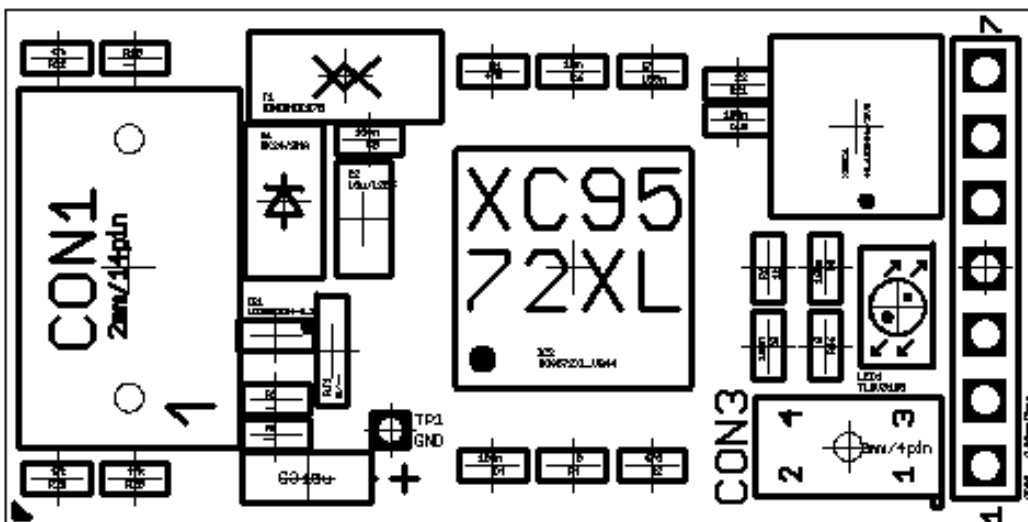
3.3. Power Suppy

The module can be powered at DIL pin 24 from 3,5 to 5,5 Volts.
Module GND pin is pin 12 in 24 pin mode, and pin 10 in 20 pin mode.
An onboard voltage regulator produces the CPLD core and I/O voltage of 3,3V.
The regulator [5] can source up to 250mA.
While it's specification allows input voltages up to 16V, power dissipation can reach it's maximum on lower input voltages, depending on the CPLD design.
However if R44 is left unmounted, the module can absorb transients up to 16V.

The module has a protection against reverse insertion, or reverse power connection.
In that case, the protection shorts the power supply by a polyfuse device.
The polyfuse recovers after deactivation of the power supply.
Burn through cycles of the polyfuse are limited.
For more information, please consult the data sheet.

Even so care should be taken when plugging the module.
Consider that a short pulse of several amps can damage the environment in which the module is inserted.

3.4. PAL / GAL Emulation Of 24 Pin And 20 Pin Devices

As a general hint, the DIL plug should be protected mechanically with the supplied DIL sockets as an adaptor.

In 24 pin mode of the module, a 24 pin socket should be used.

In 20 pin mode of the module, a 20 pin socket should be used.

Please insure, that pin 1 of the module is always pin 1 of a socket.

In the 20 pin mode, an additional GND connection must be done via a 2mm jumper on jumper block CON3 at position 1-2, see Layout Top View. This adds GND to pin 10.

In rare cases additional GND connections are desired.
Pins 3, 14 and 23 can be shorted to GND with solder jumpers JP1, JP3, JP2 respectively, on the bottom side of the module. These shorts should be soldered via a stereo microscope, to insure, that there are no other invalid connections.

4. CPLD Design Support

As for CPLD design [4] and [9] are very recommended readings.

VHDL and UCF design templates for 20 and 24 pin configurations are availlable.

5. GOP_XC9572XL I/O Voltage Levels

Since CPLD I/O's can be inputs or outputs or bidirectional, we have to distinguish between voltage levels driven from the outputs of the CPLD, and voltage levels that are applied to their inputs.

The XC9500 series inputs can accept input voltage levels from 0 to 5V, so they are 5V tolerant. However they can not deal with analog input voltages.
The maximum low input voltage VIL, where the CPLD sees a logical '0', must be 0.8V.
The minimum high input voltage VIH, where the CPLD sees a logical '1', must be 2.0V, and must not exceed 5,5V.
Voltage levels in between VIL and VIH should change very fast, transition times should be lower than 100ns, although Xilinx makes no recommendations about them in this CPLD family.

As stated in the datasheet, after configuration of the device, there are buskeepers on the I/O' s, which only allows digital levels.
However the ISE software also knows of a floating pin option, but the CPLD always has buskeepers on it's inputs and unused pins after configuration.

It is remarkable, that because of the 5V tolerant inputs, there is no diode between the inputs and VCC. So the devices can be used in hot plugging applications [6].

The XC9500 series outputs delivers different voltage levels, dependent on the supplied VCCIO voltage.
In the GOP_XC9572XL module this voltage is 3,3V.
In this case, the CPLD drives a low output '0' with a maximum of 0,4V at 8mA sink current.
If the CPLD sources current on a logical '1' output, the voltage is guaranteed to be 2,4V minimum at 4mA.
So sourcing and sinking current is not symmetrical.
If more output current is desired, [3] shows appropriate I/V curves.

Another important fact is, that a bidirectional I/O with a pullup to 5V, can not drive to 5V on the output, but 3,3V only. The output driver stage clamps the voltage to VCCIO in that case.

As an example, driving bright leds with relatively high current consumption is best done by sinking current, or in other words, the cathode of the led should be connected to a CPLD I/O, the anode to the led's supply voltage.
If the leds have forward voltages beyond 3,3V (e.g. blue leds) , the 5V tolerance can be used to completely turn off the led by tristating the output.
For driving leds with CPLD's, see also [10].

Please consider that there are 22Ω series resistors between GOP_XC9572XL pin connections and the CPLD.

6. Detailed XC9572XL-VQ44 CPLD Pinout Table

Pin	CPLD pin function *	(Schema net name) routed to	UCF port 24pin** (20 pin)	1. Comment:
1	FB1MC14 I/O/GCK3	--	gck3	Use as an internal clock node to the global clock net GCK3 If XOSC1 is used, but not routed to GCK1 or GCK2, use this global net instead.
2	FB1MC15	(PLD2) CON2 pin6	pin6 (pin6)	Connection to the 20/24pin DIL plug to pin6 via serial resistor
3	FB1MC17	(PLD3) CON2 pin7	pin7 (pin7)	Connection to the 20/24pin DIL plug to pin7 via serial resistor
4	GND	Power GND	--	Connection to the GND Layer of the PCB
5	FB3MC2	(PLD5) CON2 pin9	pin9 (pin9)	Connection to the 20/24pin DIL plug to pin9 via serial resistor
6	FB3MC5	(PLD6) CON2 pin8	pin8 (pin8)	Connection to the 20/24pin DIL plug to pin8 via serial resistor
7	FB3MC8	(PRG_GND) Power GND	--	Additional GND connection as a programmable ground pin
8	FB3MC9	(LED_G) LED1	ledgn	Green led of the duo led 0 -> led off, 1 -> led on
9	TDI	(TDI) CON1 pin10	--	JTAG interface, additional 47k pullup to VCC
10	TMS	(TMS) CON1 pin4	--	JTAG interface, additional 47k pullup to VCC
11	TCK	(TCK) CON1 pin6	--	JTAG interface, additional 47k pullup to VCC
12	FB3MC11	(PLD12) CON2 pin10	pin10 (--)	Connection to the 24pin DIL plug to pin10 via serial resistor Short to GND by CON3 for 20pin DIL plug
13	FB3MC14	(PLD13) CON2 pin11	pin11 (--)	Connection to the 24pin DIL plug to pin11 via serial resistor Not used for the 20pin DIL plug
14	FB3MC15	(PLD14) CON4 pin3	tp3	Test connector pin3
15	VCCINT	Power VCC	--	Power supply 3,3V from regulator LP2992-3.3
16	FB3MC17	(RC_IN) RC network	rcin	Input to an RC network, this is for demonstration, that rc oscillators do not work reliably with XC9500, but on CoolRunner-II devices with Schmitt Trigger inputs.
17	GND	Power GND	--	Connection to the GND Layer of the PCB
18	FB3MC16	(RC_OUT) RC network	rcout	Output from an RC network, this is for demonstration, that rc oscillators do not work reliably with XC9500, but on CoolRunner-II devices with Schmitt Trigger inputs
19	FB4MC2	(PLD19) CON4 pin4	tp4	Test connector pin4
20	FB4MC5	(PLD20) CON4 pin5	tp5	Test connector pin5
21	FB4MC8	(PLD21) CON4 pin6	tp6	Test connector pin6 R44 could be soldered to the 5V supply voltage, for generation of an 5V rail on tp6. Use 680Ω to 10kΩ for R44
22	FB4MC11	(PLD22) CON2 pin14	pin14 (--)	Connection to the 24pin DIL plug to pin14 via serial resistor Not used for the 20pin DIL plug
23	FB4MC14	(OSC) XOSC1	osc	Crystal oscillator input This signal should be routed internally to a global clock net
24	TDO	(TDO)	--	JTAG interface

		CON1 pin8		
25	GND	Power GND	--	Connection to the GND Layer of the PCB
26	VCCIO	Power VCC	--	Power supply 3,3V from regulator LP2992-3.3
27	FB4MC15	(PLD27) CON2 pin15	pin15 (pin11)	Connection to the 24pin DIL plug to pin15 via serial resistor Connection to the 20pin DIL plug to pin11 via serial resistor
28	FB4MC17	(PLD28) CON2 pin16	pin16 (pin12)	Connection to the 24pin DIL plug to pin16 via serial resistor Connection to the 20pin DIL plug to pin12 via serial resistor
29	FB2MC2	(PLD29) CON2 pin17	pin17 (pin13)	Connection to the 24pin DIL plug to pin17 via serial resistor Connection to the 20pin DIL plug to pin13 via serial resistor
30	FB2MC5	(PLD30) CON2 pin18	pin18 (pin14)	Connection to the 24pin DIL plug to pin18 via serial resistor Connection to the 20pin DIL plug to pin14 via serial resistor
31	FB2MC6	(PLD31) CON2 pin19	pin19 (pin15)	Connection to the 24pin DIL plug to pin19 via serial resistor Connection to the 20pin DIL plug to pin15 via serial resistor
32	FB2MC8	(PLD32) CON2 pin20	pin20 (pin16)	Connection to the 24pin DIL plug to pin20 via serial resistor Connection to the 20pin DIL plug to pin16 via serial resistor
33	FB2MC9 I/O/GSR	(LED_R) LED1	ledrd	Red led of the duo led 0 -> led off, 1 -> led on This is also an input to the global set/reset net GSR
34	FB2MC11 I/O/GTS2	(PLD34) CON4 pin2	tp2	Test connector pin2, R38 is soldered to the 3,3V supply voltage, as a pullup on tp2. Tp2 can be used as a simple input by shorting to tp1 This is also an input to the global tri state net GTS2
35	VCCINT	Power VCC	--	Power supply 3,3V from regulator LP2992-3.3
36	FB2MC14 I/O/GTS1	(PLD36) CON2 pin13	pin13 (--)	Connection to the 24pin DIL plug to pin13 via serial resistor Not used for the 20pin DIL plug This is also an input to the global tri state net GTS1
37	FB2MC15	(PLD37) CON2 pin21	pin21 (pin17)	Connection to the 24pin DIL plug to pin21 via serial resistor Connection to the 20pin DIL plug to pin17 via serial resistor
38	FB2MC17	(PLD38) CON2 pin22	pin22 (pin18)	Connection to the 24pin DIL plug to pin22 via serial resistor Connection to the 20pin DIL plug to pin18 via serial resistor
39	FB1MC2	(PLD39) CON2 pin23	pin23 (pin19)	Connection to the 24pin DIL plug to pin23 via serial resistor Connection to the 20pin DIL plug to pin19 via serial resistor
40	FB1MC5	(PLD40) CON2 pin3	pin3 (pin3)	Connection to the 20/24pin DIL plug to pin3 via serial resistor
41	FB1MC6	(PLD41) CON2 pin4	pin4 (pin4)	Connection to the 20/24pin DIL plug to pin4 via serial resistor
42	FB1MC8	(PLD42) CON2 pin5	pin5 (pin5)	Connection to the 20/24pin DIL plug to pin5 via serial resistor
43	FB1MC9 I/O/GCK1	(PLD43) CON2 pin10	pin1 (pin1)	Connection to the 20/24pin DIL plug to pin1 via serial resistor This is also an input to the global clock net 1 GCK1
44	FB1MC11 I/O/GCK2	(PLD44) CON2 pin10	pin2 (pin2)	Connection to the 20/24pin DIL plug to pin2 via serial resistor This is also an input to the global clock net 2 GCK2

* FB1MC11 denotes function block1, macrocell 11
** There is an UCF file definition for 24pin, and another one for 20pin device usage

7. CON4 Test Connector Pinout Table

Pin	CPLD pin function *	(Schema net name) routed to	UCF port name **	Comment
1	GND	GND	--	Power ground plane connection
2	FB2MC11 I/O/GTS2	(PLD34) CON4 pin2	tp2	Test connector pin2, R38 is soldered to the 3,3V supply voltage, as a pullup on tp2. Tp2 can be used as a simple input by shorting to tp1 This is also an input to the global tri state net GTS2
3	FB3MC15	(PLD14) CON4 pin3	tp3	Test connector pin3
4	FB4MC2	(PLD19) CON4 pin4	tp4	Test connector pin4
5	FB4MC5	(PLD20) CON4 pin5	tp5	Test connector pin5
6	FB4MC8	(PLD21) CON4 pin6	tp6	Test connector pin6 R44 could be soldered to the 5V supply voltage, for generation of an 5V rail on tp6. Use 680Ω to 10kΩ for R44
7	--	(VCC_IN) voltage reg	--	5V input voltage protected by a polyfuse

8. CON3 Configuration Jumper options

1-2	Enable 20pin PAL / GAL Emulation, put GND to pin 10 of CON2
3-4	Enable XOSC1 crystal oscillator 49,152 MHz

9. CON2 DIL Connector Pinout Table

| Pin	CPLD pin function *	(Schema net name) routed to	UCF port name **	Comment
1	FB1MC9 I/O/GCK1	(PLD43) CPLD pin 43	pin1 (pin1)	Connection to CPLD pin 43 via serial resistor This is also an input to the global clock net 1 GCK1
2	FB1MC11 I/O/GCK2	(PLD44) CPLD pin 44	pin2 (pin2)	Connection to CPLD pin 44 via serial resistor This is also an input to the global clock net 2 GCK2
3	FB1MC5	(PLD40) CPLD pin 40	pin3 (pin3)	Connection to CPLD pin 40 via serial resistor
4	FB1MC6	(PLD41) CPLD pin 41	pin4 (pin4)	Connection to CPLD pin 41 via serial resistor
5	FB1MC8	(PLD42) CPLD pin 42	pin5 (pin5)	Connection to CPLD pin 42 via serial resistor
6	FB1MC15	(PLD2) CPLD pin 2	pin6 (pin6)	Connection to CPLD pin 2 via serial resistor
7	FB1MC17	(PLD3) CPLD pin 3	pin7 (pin7)	Connection to CPLD pin 3 via serial resistor
8	FB3MC5	(PLD6) CPLD pin 6	pin8 (pin8)	Connection to CPLD pin 6 via serial resistor
9	FB3MC2	(PLD5) CPLD pin 5	pin9 (pin9)	Connection to CPLD pin 5 via serial resistor
10	FB3MC11	(PLD12) CPLD pin 12	pin10 (--)	Connection to CPLD pin 12 via serial resistor Short to GND by CON3 for 20pin DIL plug
11	FB3MC14	(PLD13) CPLD pin 13	pin11 (--)	Connection to CPLD pin 13 via serial resistor Not used for the 20pin DIL plug
12	GND	GND	--	Power ground plane connection
13	FB2MC14 I/O/GTS1	(PLD36) CPLD pin 36	pin13 (--)	Connection to CPLD pin 36 via serial resistor Not used for the 20pin DIL plug This is also an input to the global tri state net GTS1
14	FB4MC11	(PLD22) CPLD pin 22	pin14 (--)	Connection to CPLD pin 22 via serial resistor Not used for the 20pin DIL plug
15	FB4MC15	(PLD27) CPLD pin 27	pin15 (pin11)	Connection to CPLD pin 27 via serial resistor
16	FB4MC17	(PLD28) CPLD pin 28	pin16 (pin12)	Connection to CPLD pin 28 via serial resistor
17	FB2MC2	(PLD29) CPLD pin 29	pin17 (pin13)	Connection to CPLD pin 29 via serial resistor
18	FB2MC5	(PLD30) CPLD pin 30	pin18 (pin14)	Connection to CPLD pin 30 via serial resistor
19	FB2MC6	(PLD31) CPLD pin 31	pin19 (pin15)	Connection to CPLD pin 31 via serial resistor
20	FB2MC8	(PLD32) CPLD pin 32	pin20 (pin16)	Connection to CPLD pin 32 via serial resistor
21	FB2MC15	(PLD37) CPLD pin 37	pin21 (pin17)	Connection to CPLD pin 37 via serial resistor
22	FB2MC17	(PLD38) CPLD pin 38	pin22 (pin18)	Connection to CPLD pin 38 via serial resistor
23	FB1MC2	(PLD39) CPLD pin 39	pin23 (pin19)	Connection to CPLD pin 39 via serial resistor

| 24 | -- | PIN_24 | -- | 5V input voltage to the module |

10. DIL Connector Layout

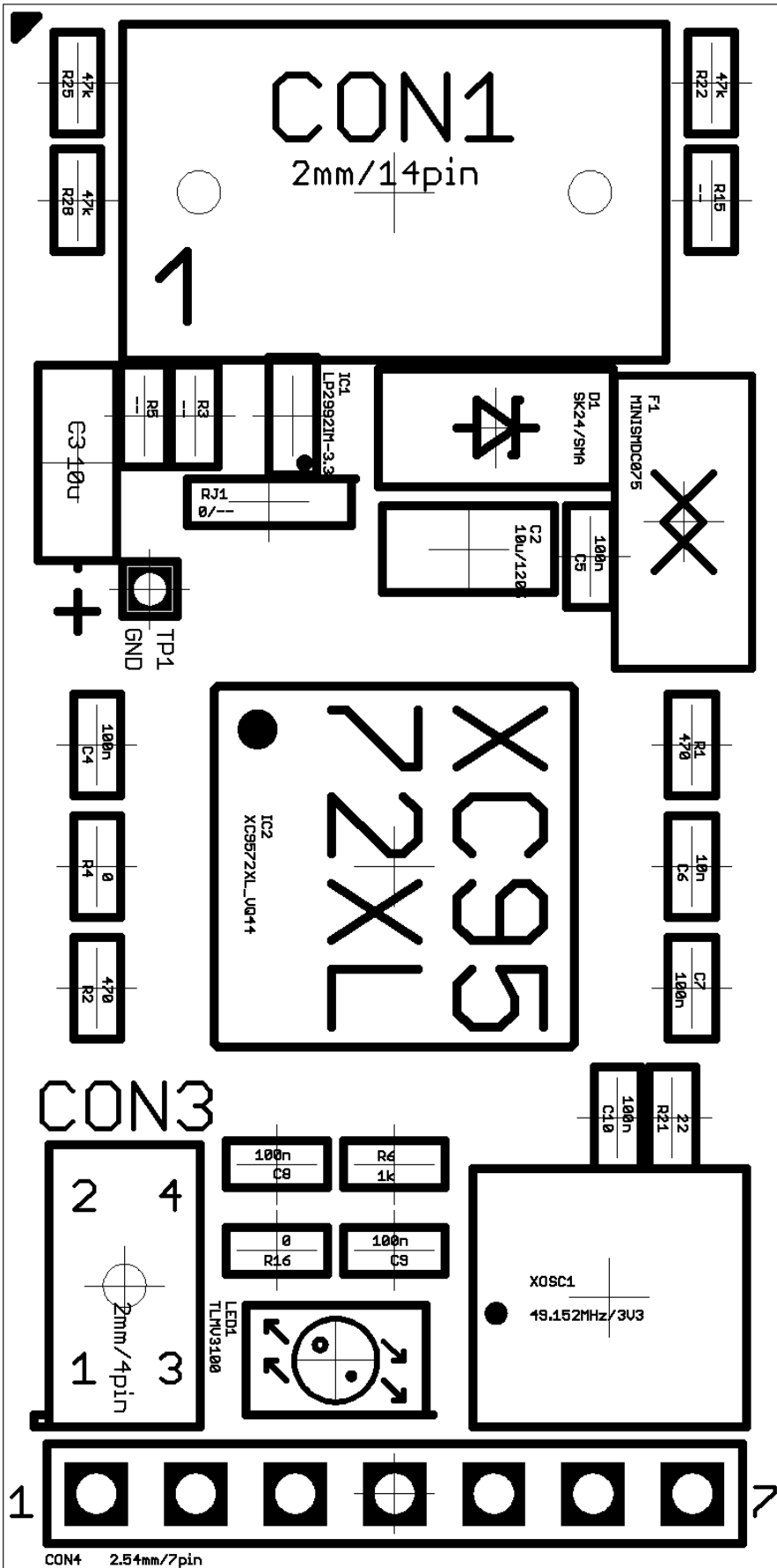GOP_XC9572XL module top view for 24 pin and 20 pin emulation mode:
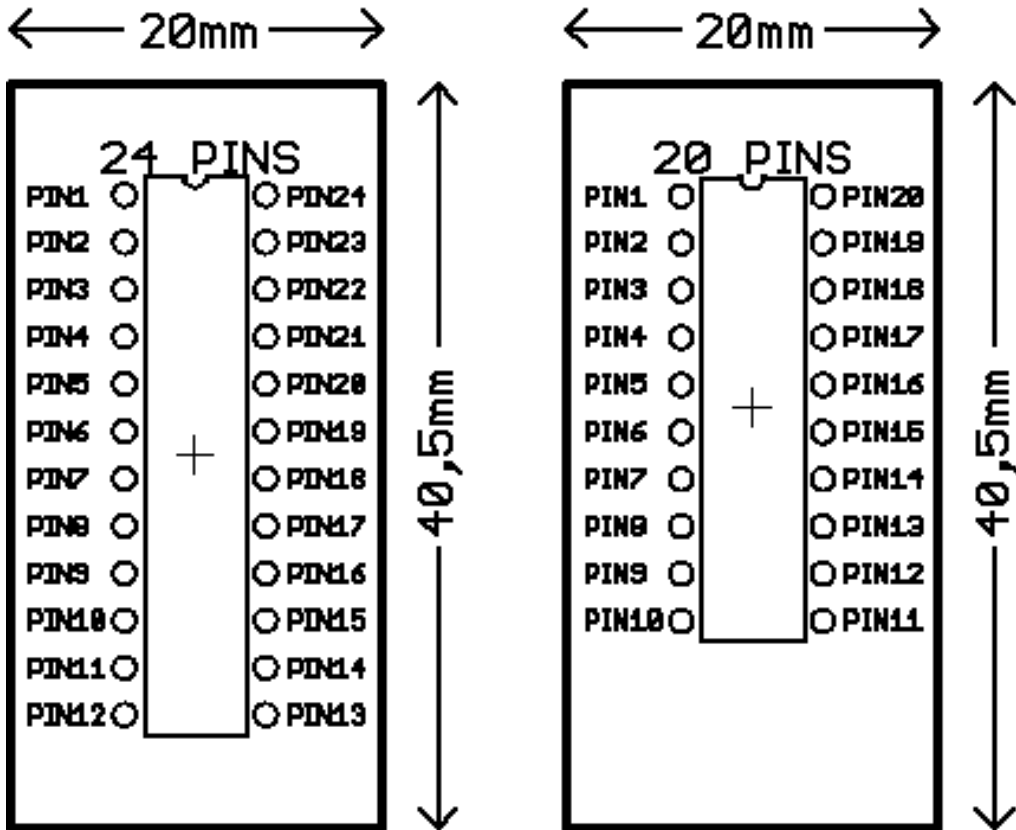
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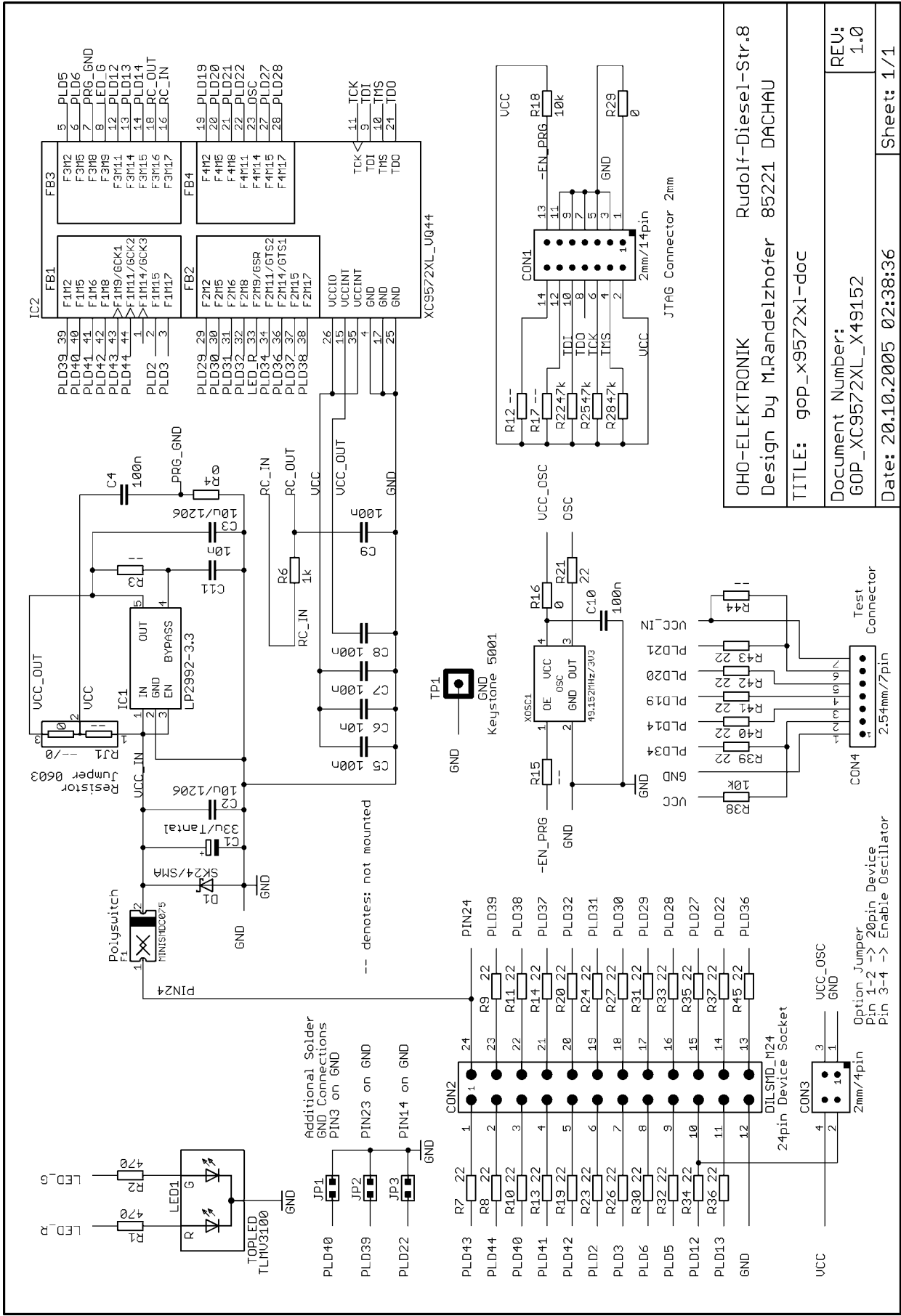
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Design by M.Randelzhofer   85221 DACHAU
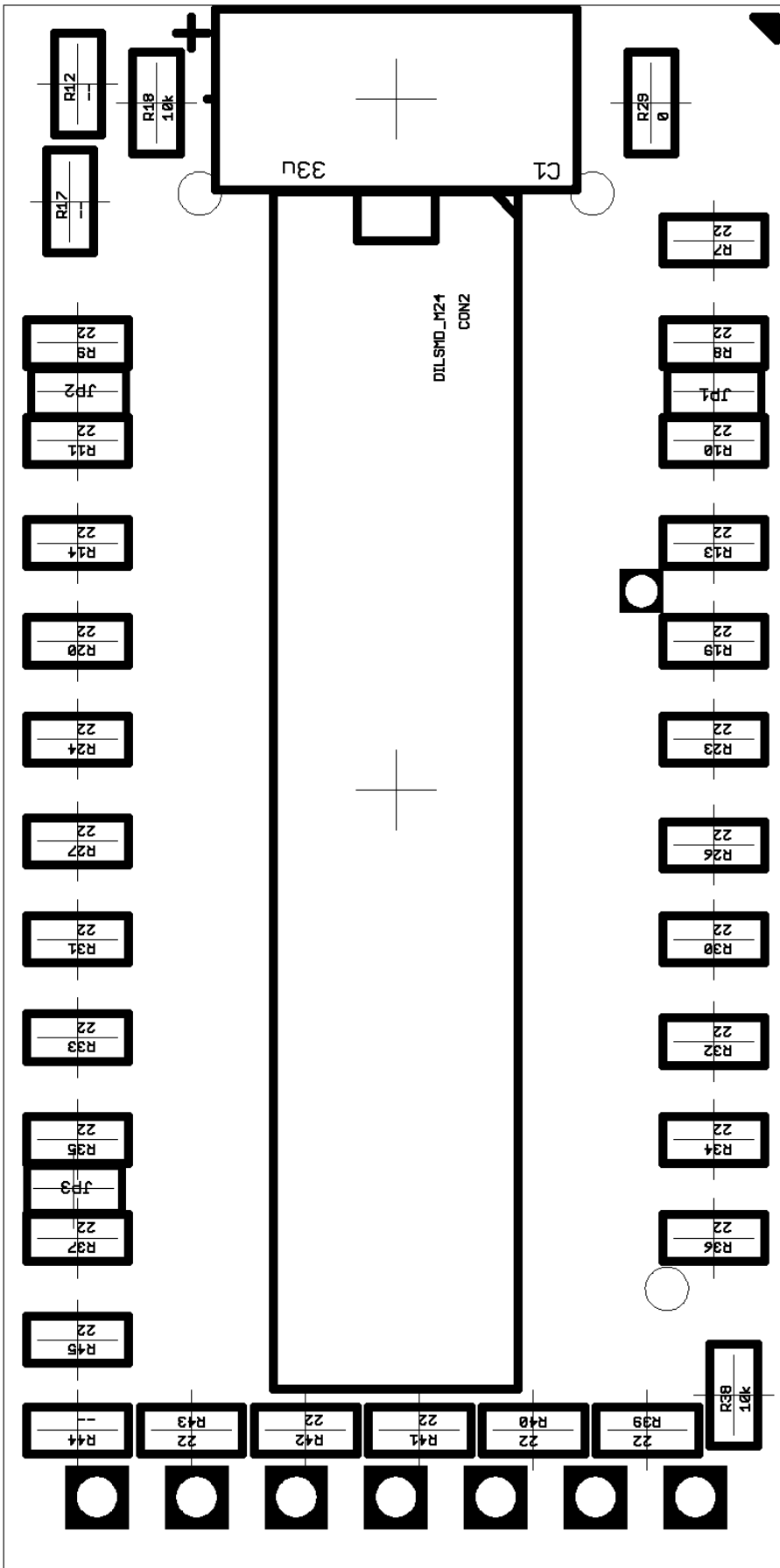
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GOP_XC9572XL_X49152

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Sheet: 1/1

12. Module Layout Top View

CON1
2mm/14pin

1

R25 47k
R28 47k
R22 47k
R15 --

C3 10u
R5 --
R3 --
IC1 LP2992IM-3.3
RJ1 0/--
D1 SK24/SMA
F1 MINISMDC075
C2 10u/120
C5 100n

TP1 GND
+

C4 100n
R4 0
R2 470
IC2 XC9572XL_VQ44
XC95 72XL
R1 470
C6 10n
C7 100n

CON3

2 4
1 3
2mm/4pin

C8 100n
R6 1k
R16 0
C9 100n
LED1 TLMU3100

C10 100n
R21 22

XOSC1
49.152MHz/3V3

1   7
CON4   2.54mm/7pin

13. Module Layout Bottom View

14. Technical Specifications

CPLD:	Xilinx XC9572XL-10VQ44C
Supply Voltage on PIN24:	3,5 - 5,5V
Size:	40,5 x 20mm, 1,594" x 0,787"
Height PCB to Top:	max. 8mm, 0,315"
Height PCB to Bottom:	max. 12mm, 0,472"
Weight:	7g

15. Literature

- [1] DS054 XC9500XL High-Performance CPLD Family Data Sheet
  http://direct.xilinx.com/bvdocs/publications/DS054.pdf

- [2] DS057 XC9572XL High Performance CPLD
  http://direct.xilinx.com/bvdocs/publications/ds057.pdf

- [3] XAPP150 I/V Curves for Xilinx FPGA and CPLD Families
  http://direct.xilinx.com/bvdocs/appnotes/xapp150.pdf

- [4] XAPP444 CPLD Fitting, Tips and Tricks
  http://direct.xilinx.com/bvdocs/appnotes/xapp444.pdf

- [5] LP2992 Micropower 250 mA Low-Noise Ultra Low-Dropout Regulator
  http://cache.national.com/ds/LP/LP2992.pdf

- [6] XAPP140 XC9500XL CPLD Power Sequencing and Hot Plugging
  http://direct.xilinx.com/bvdocs/appnotes/xapp140.pdf

- [7] DS097 Xilinx Parallel Cable IV
  http://direct.xilinx.com/bvdocs/publications/ds097.pdf

- [8] DS300 Platform Cable USB
  http://direct.xilinx.com/bvdocs/publications/ds300.pdf

- [9] XAPP784 Bulletproof CPLD Design Practices
  http://direct.xilinx.com/bvdocs/appnotes/xapp784.pdf

- [10] XAPP805 Driving Leds with Xilinx CPLD's
  http://direct.xilinx.com/bvdocs/appnotes/xapp805.pdf

16.   USER'S MANUAL Revisions

Version	Date	Comments
V0.9	23/10/2005	Prerelease